CLAIMS

Sub A2

1. A method for regenerating a clock signal based on a flip-flop and on two complementary signals at the clock rate, the flip-flop being connected as a divider by two of a combination of shaping signals each translating a direction, respectively rising or falling, of the edges of one of the complementary signals, wherein one of said shaping signals is used to reset the flip-flop.

2. The method of claim 1, applied to regenerating a clock signal downstream of a capacitive isolation barrier carrying the two complementary signals.

3. The method of claim 2, wherein an output of the flip-flop provides an image of a first one of said complementary signals, the flip-flop being reset on edges of the shaping signal of the other complementary signal.

4. A circuit for regenerating a clock signal based on two complementary signals by means of a D flip-flop, a clock input of which receives the result of a logic combination of two shaping signals resulting from a filtering of the respective rising edges of the complementary signals, wherein a reset input of the flip-flop receives one of said shaping signals.

5. The circuit of claim 4, wherein the logic combination is of NAND type, the shaping signals being provided by inverters.

6. The circuit of claim 5, wherein the reset input of the flip-flop is connected at the output of the inverter for shaping the complementary signal, of which an output of the flip-flop provides an inverted image.

7. An interface system between a modem and a transmission line, of the type using a capacitive isolation barrier to transmit a clock for modulating the signals to be transmitted from the modem to a processing circuit on the line side, including the clock regeneration circuit of claim 4.

add A2